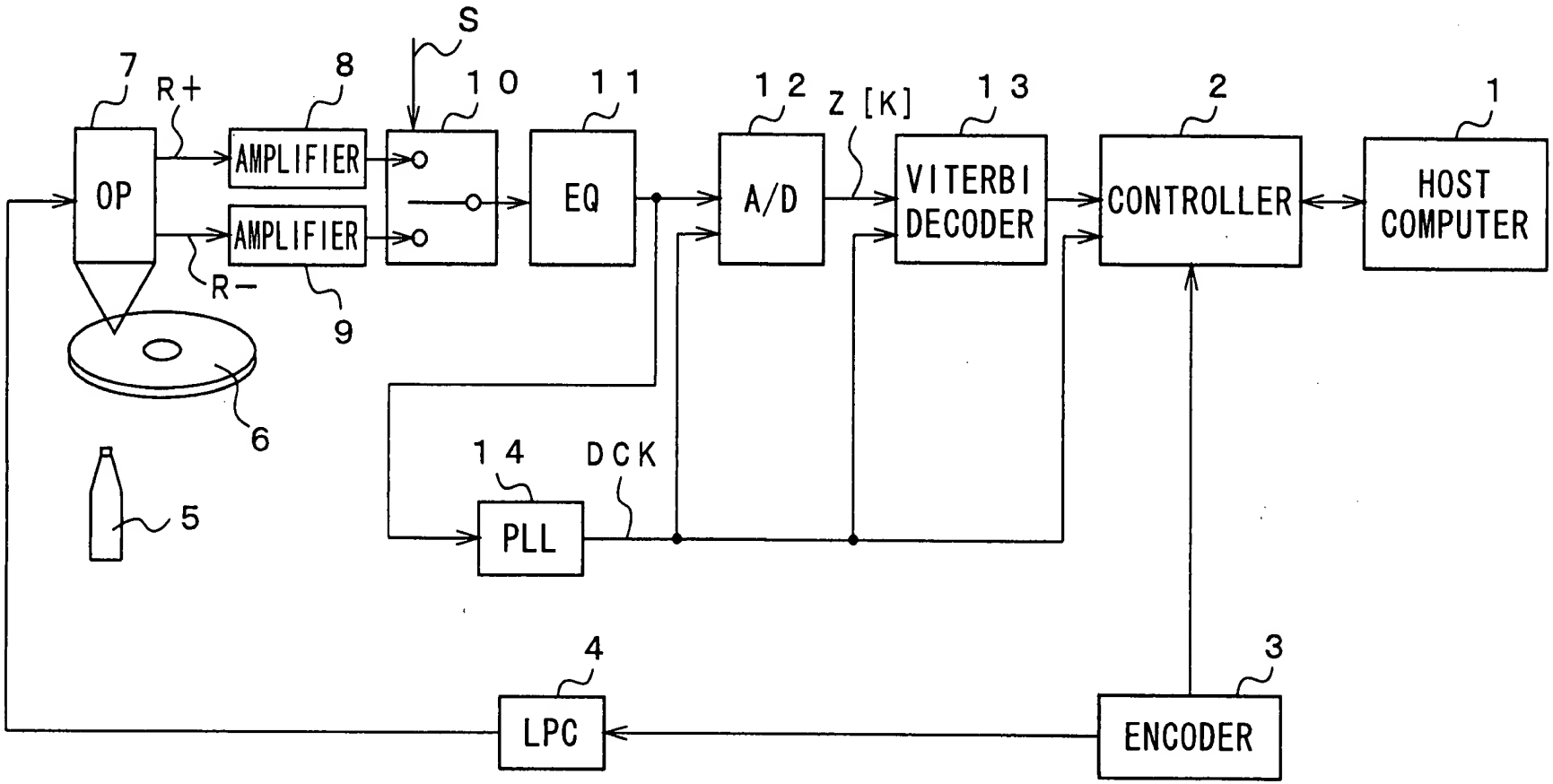
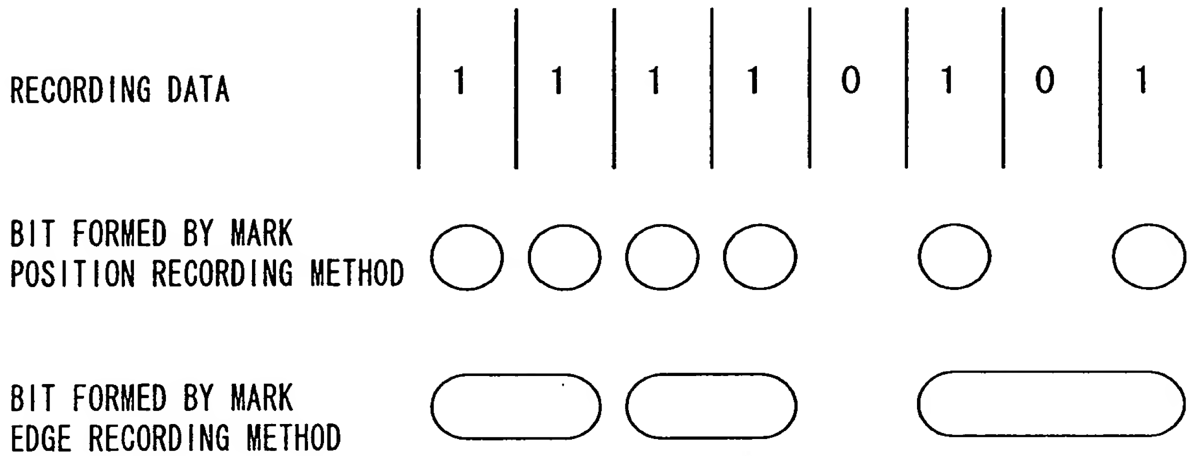
FIG. 1


7
R+
8
S
10
11
12
Z [K]
13
2
1
OP
AMPLIFIER
AMPLIFIER
EQ
A/D
VITERBI DECODER
CONTROLLER
HOST COMPUTER
R−
9
6
5
14
DCK
PLL
4
3
LPC
ENCODER

F I G. 2


RECORDING DATA
1 1 1 1 0 1 0 1
BIT FORMED BY MARK
POSITION RECORDING METHOD
BIT FORMED BY MARK
EDGE RECORDING METHOD

F I G. 7

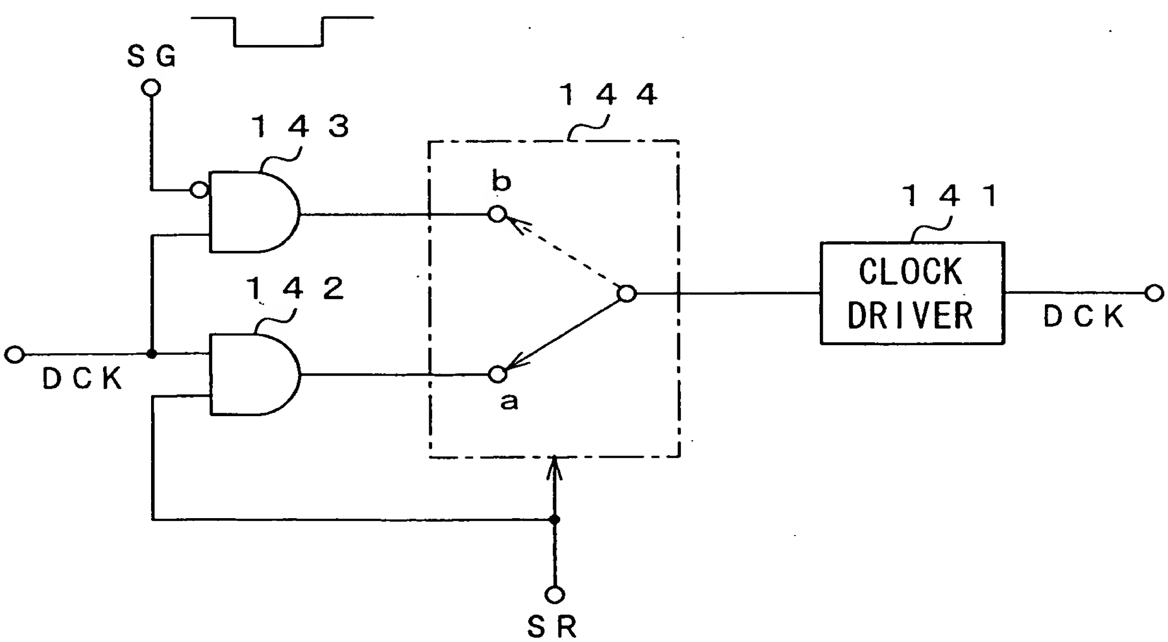

SG
143
142
144
b
a
141
CLOCK
DRIVER
DCK
DCK
SR

FIG. 3

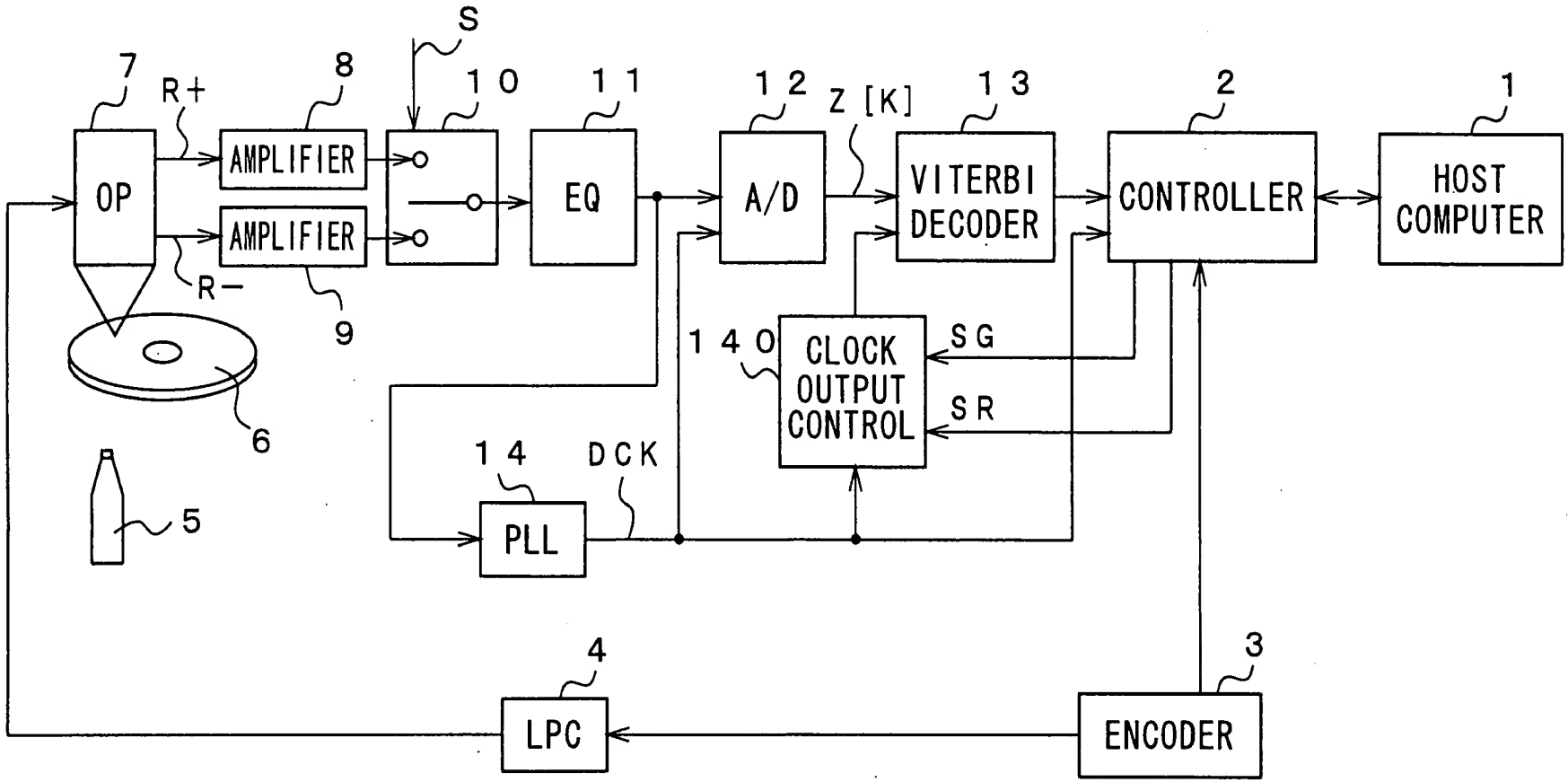

S
7
R+
8
10
11
12
Z [K]
13
2
1
OP
AMPLIFIER
AMPLIFIER
EQ
A/D
VITERBI DECODER
CONTROLLER
HOST COMPUTER
R−
9
140
CLOCK OUTPUT CONTROL
SG
SR
6
14
DCK
5
PLL
4
3
LPC
ENCODER

FIG. 4

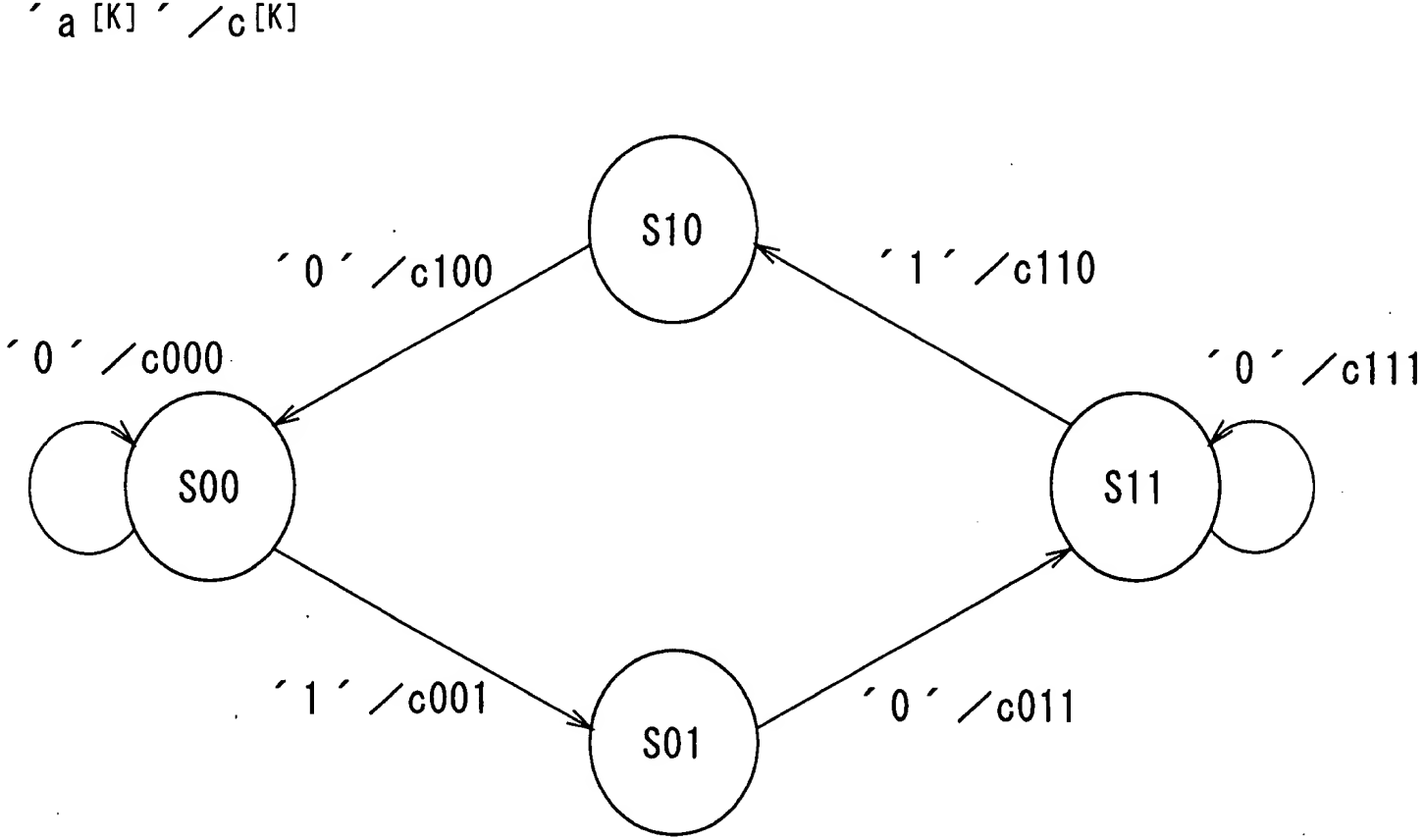


FIG. 5

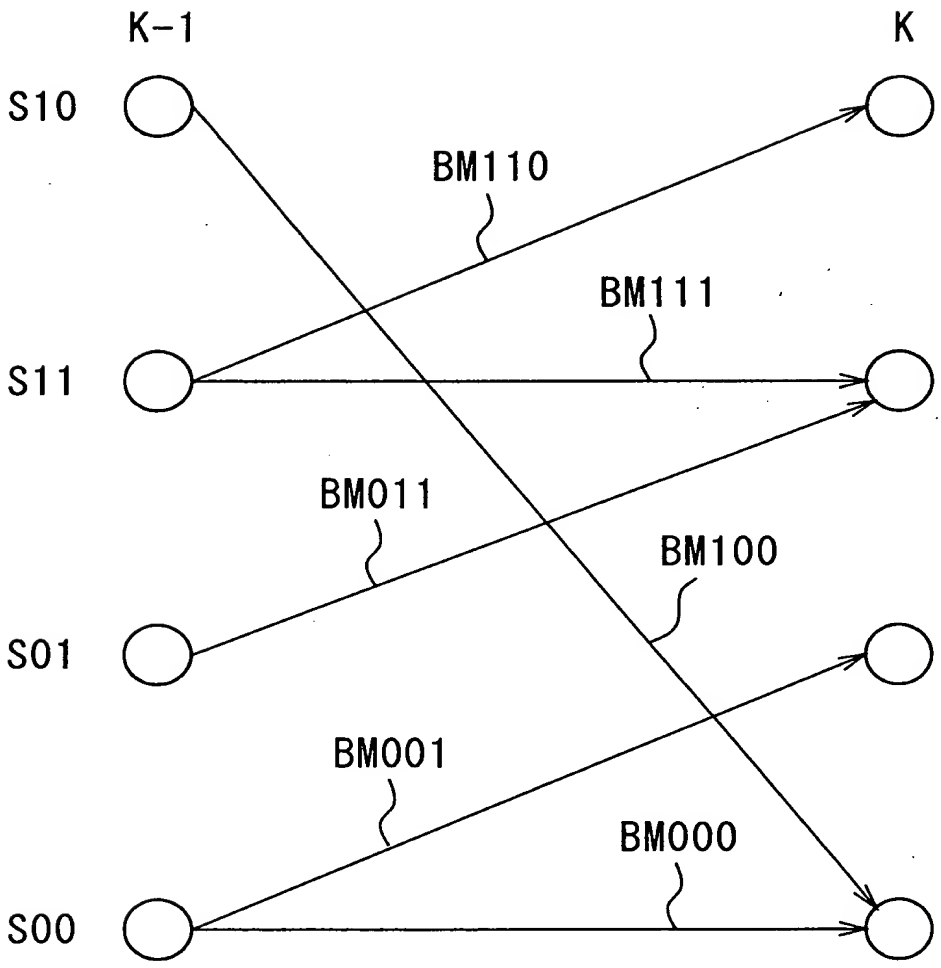


FIG. 6

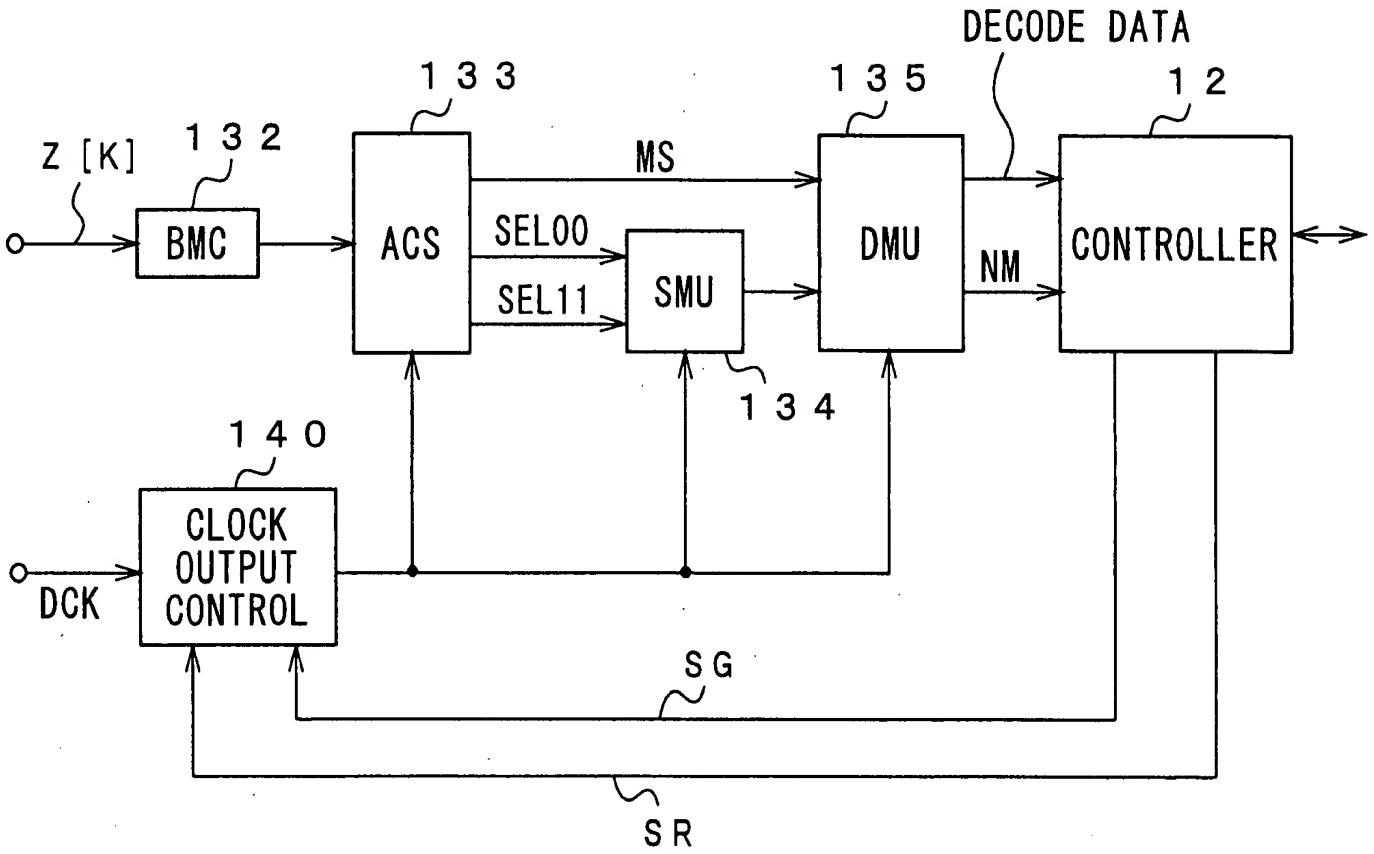

DECODE DATA
133
135
12
Z [K]
132
MS
BMC
ACS
SEL00
SEL11
SMU
DMU
NM
CONTROLLER
134
140
CLOCK
OUTPUT
CONTROL
DCK
SG
SR

FIG. 8

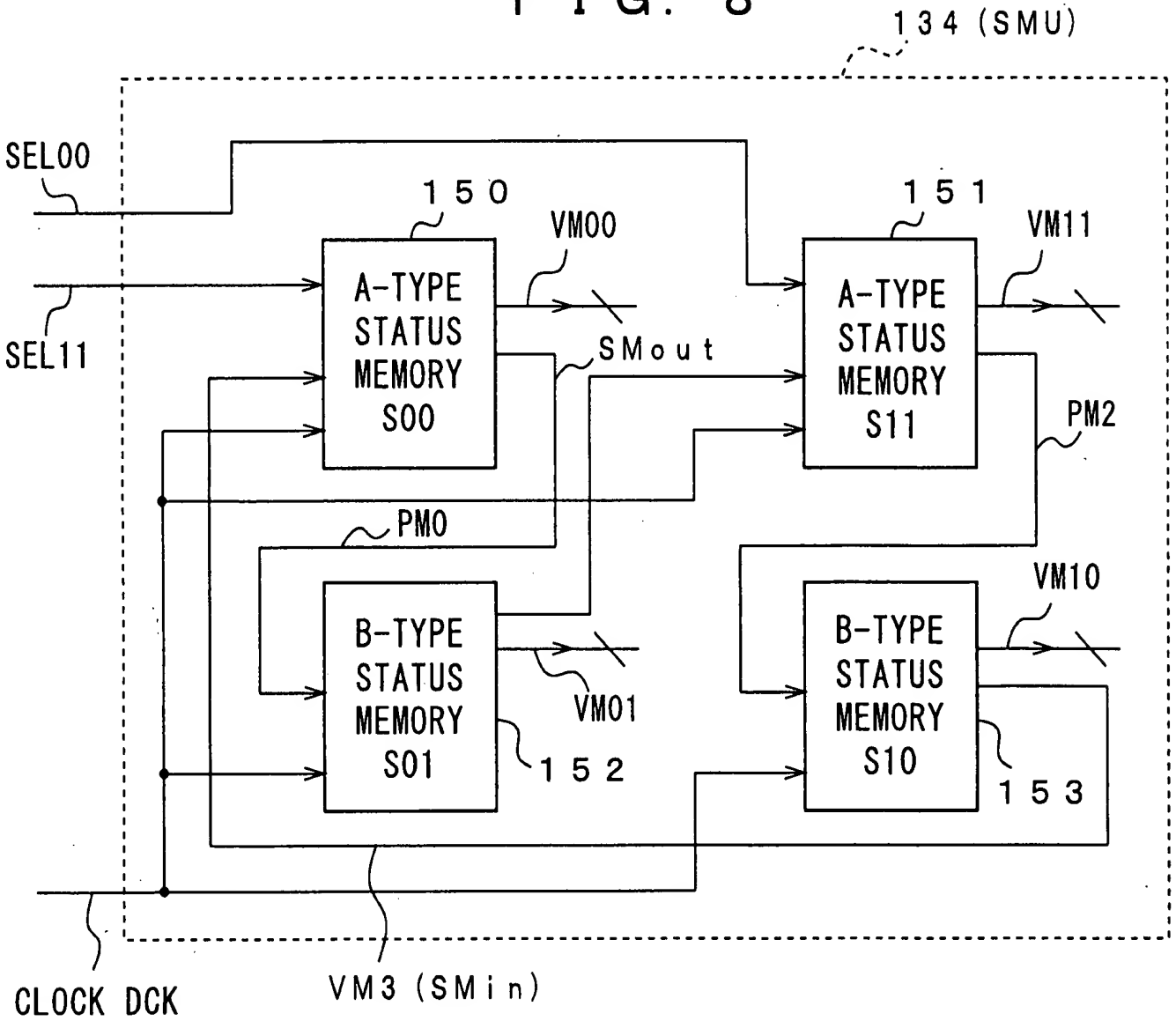

134 (SMU)
SEL00
SEL11
150
151
VM00
VM11
A-TYPE STATUS MEMORY S00
A-TYPE STATUS MEMORY S11
SMout
PM2
PM0
VM10
B-TYPE STATUS MEMORY S01
B-TYPE STATUS MEMORY S10
VM01
152
153
CLOCK DCK
VM3 (SMin)

FIG. 9

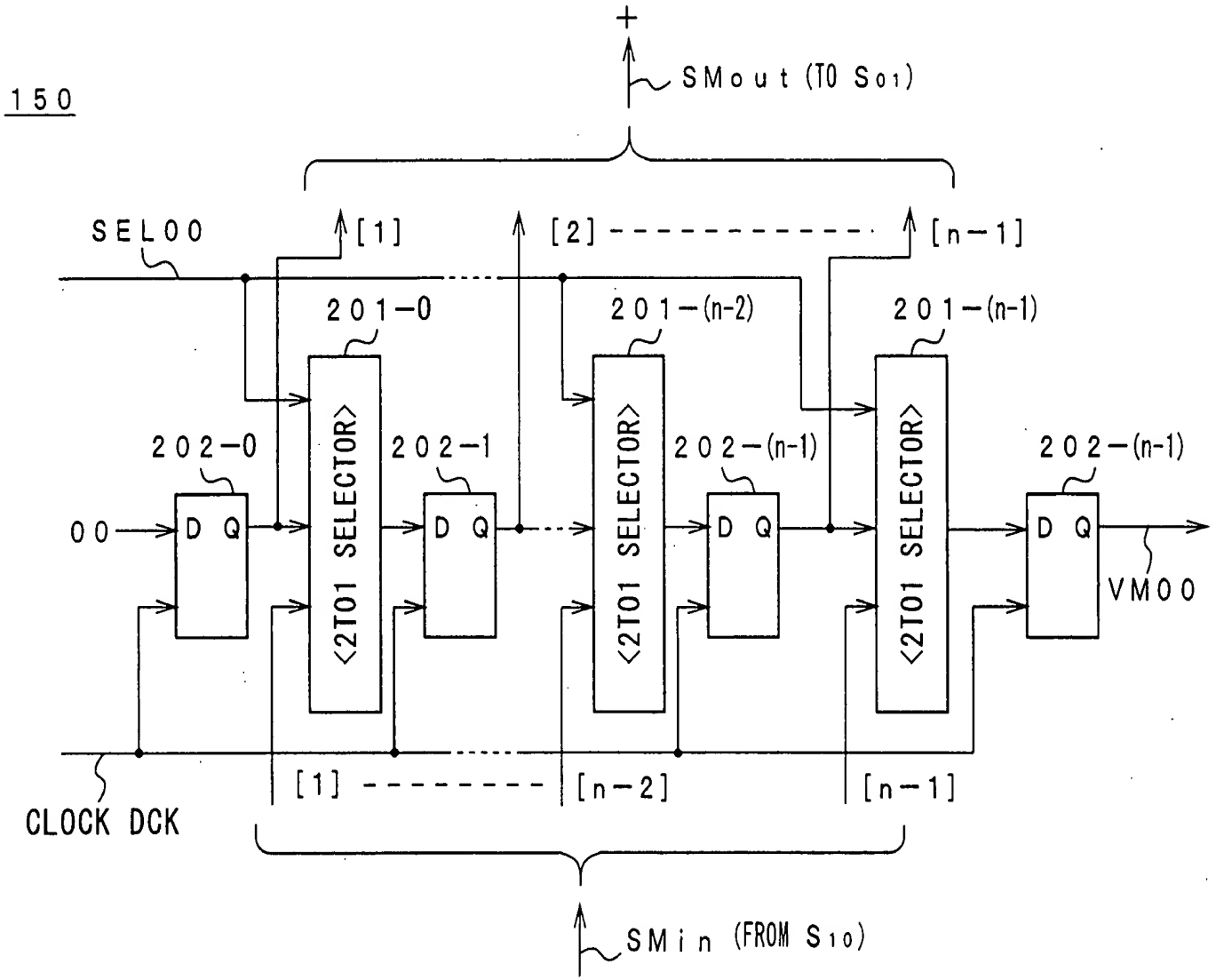
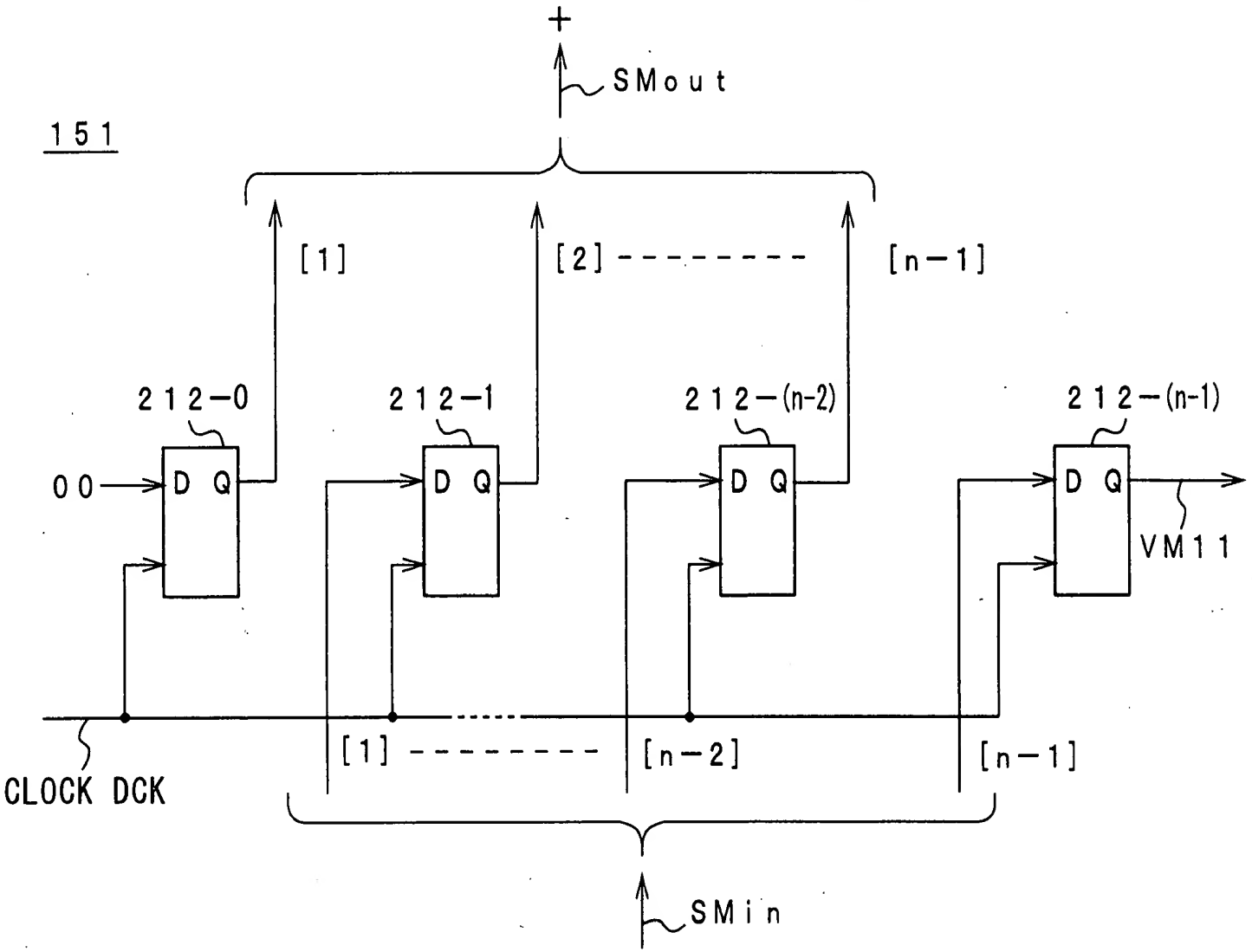

150
SMout (TO S01)
SEL00
[1]
[2]
[n-1]
201-0
201-(n-2)
201-(n-1)
202-0
202-1
202-(n-1)
202-(n-1)
00
D Q
<2TO1 SELECTOR>
VM00
CLOCK DCK
[1]
[n-2]
[n-1]
SMin (FROM S10)

FIG. 10


SMout
151
[1]
[2]
[n−1]
212−0
212−1
212−(n-2)
212−(n-1)
00
D Q
VM11
CLOCK DCK
[1]
[n−2]
[n−1]
SMin

F I G. 1 1

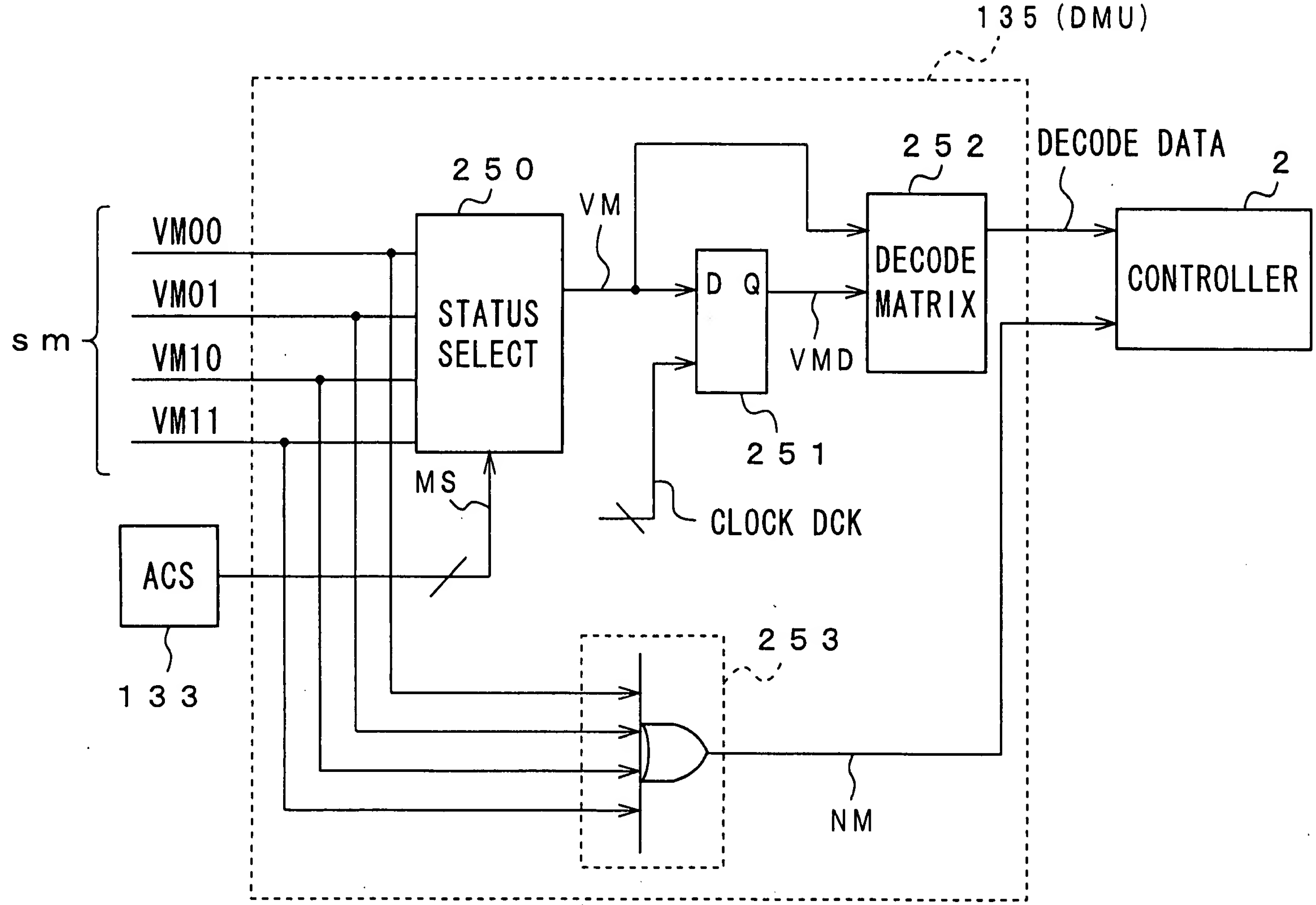

135 (DMU)
sm
VM00
VM01
VM10
VM11
ACS
133
250
STATUS SELECT
MS
VM
D Q
251
CLOCK DCK
VMD
252
DECODE MATRIX
DECODE DATA
2
CONTROLLER
253
NM

FIG. 12

MS	VM
00	VM00
01	VM01
10	VM11
11	VM10

FIG. 13

VMD	VM	DECODE DATA VALUE
00	00 01	0 1
01	11	0
11	11 10	0 1
10	00	0